Automotive MOSFETs

Data Sheet Explanation

Application Note

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01/2014	V1.1	MP	Update of formula 1
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1 Abstract

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This Application Note is intended to provide an explanation of the parameters and diagrams given in the datasheet of automotive low voltage MOSFETs. With the application note the designer of ECUs requiring a low voltage MOSFET is able to use the datasheet in the right way and will be provided with background information.

2 Introduction

Each parameter mentioned in the datasheet gives values which characterizes the device as detailed as possible.

With this information the designer should be able on the one hand to compare devices from different competitors with each other; on the other hand the information should be sufficient to figure out where the limits of the device are.

This document helps to understand the datasheet parameter and characteristics much better. It explains the interaction between the parameters and the influence of the conditions as temperature or gate voltage.

3 Datasheet Parameters

The attached diagrams, tables and explanations are referring to the datasheet of IPD90N06S4-04 (rev.1.0 from 2008-03-7) as example. The shown values and characteristics are not feasible to use for design-in activities. For the latest version of datasheets please refer to our webpage (www.infineon.com/optimos-T).

3.1 Power dissipation

This parameter describes the maximum feasible power dissipation over the case temperature (Figure 1, Figure 2).

The power dissipation of the MOSFET is directly related to the chip size of the device (eq.(1)). Up to a junction temperature of 25°C, the power dissipation is specified at its maximum value (eq.(2)). With increasing case temperature the power dissipation is decreasing according to:

(1) $$P_{tot}(T_C) = \frac{T_J - T_C}{R_{thJC}}$$

(2) $$P_{tot}(\max) = \frac{(175-25)K}{0.8\,K/W} = 188W$$

Power dissipation	P_{tot}	T_C=25°C	188	W

Figure 1 Maximum ratings for P_{tot} (datasheet)

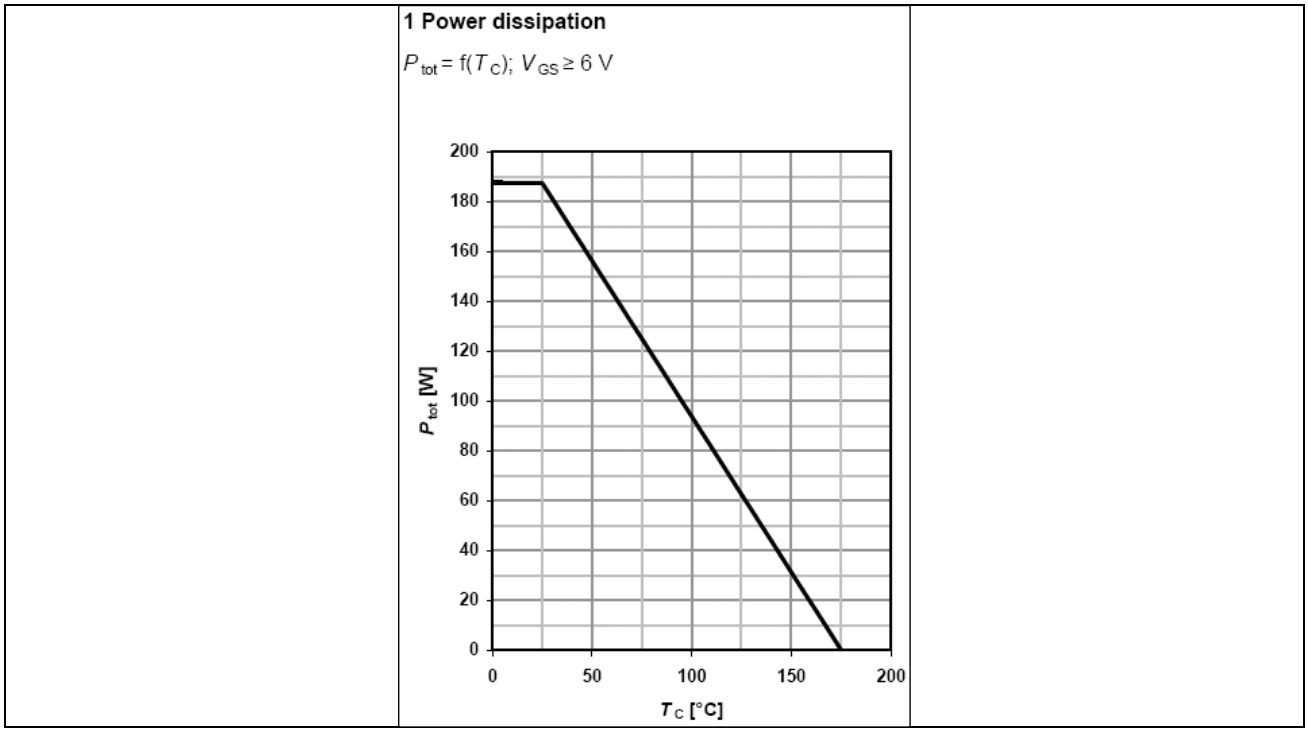

Figure 2 Power dissipation P_{tot} = f(T_C)

3.2 Drain current

The datasheet specifies a maximum continuous drain current I_D and a pulsed drain current $I_{D,pulse}$ (Figure 3). The maximum continuous drain current depends on the maximum power dissipation (chapter 3.1) and is defined by the temperature difference junction to case, the thermal resistance R_{thJC} and the on-state resistance $R_{DS(on)}$ at maximum junction temperature (eq.(3)). Please refer to chapter 3.8 for calculating the temperature dependency of the on-state resistance.

(3) $$I_D(T_C) = \sqrt{\frac{\frac{T_J - T_C}{R_{thJC}}}{R_{DS(on)\_TJ(\max)}}} \qquad I_D(\max) = \sqrt{\frac{\frac{(175-25)K}{0.8\,K/W}}{6.6m\Omega}} = 169A$$

Additional boundary conditions as bondwire diameter, chip design and assembly are limiting the maximum drain current to the given value (Figure 4).

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current[1]	I_D	T_C=25°C, V_{GS}=10V	90	A
		T_C=100°C, V_{GS}=10V[2]	90	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25°C	360	

[1] Current is limited by bondwire; with an R_{thJC} = 0.8K/W the chip is able to carry 169A at 25°C. For detailed information see Application Note ANPS071E

[2] Defined by design. Not subject to production test.

Figure 3 Maximum ratings for I_D (datasheet)

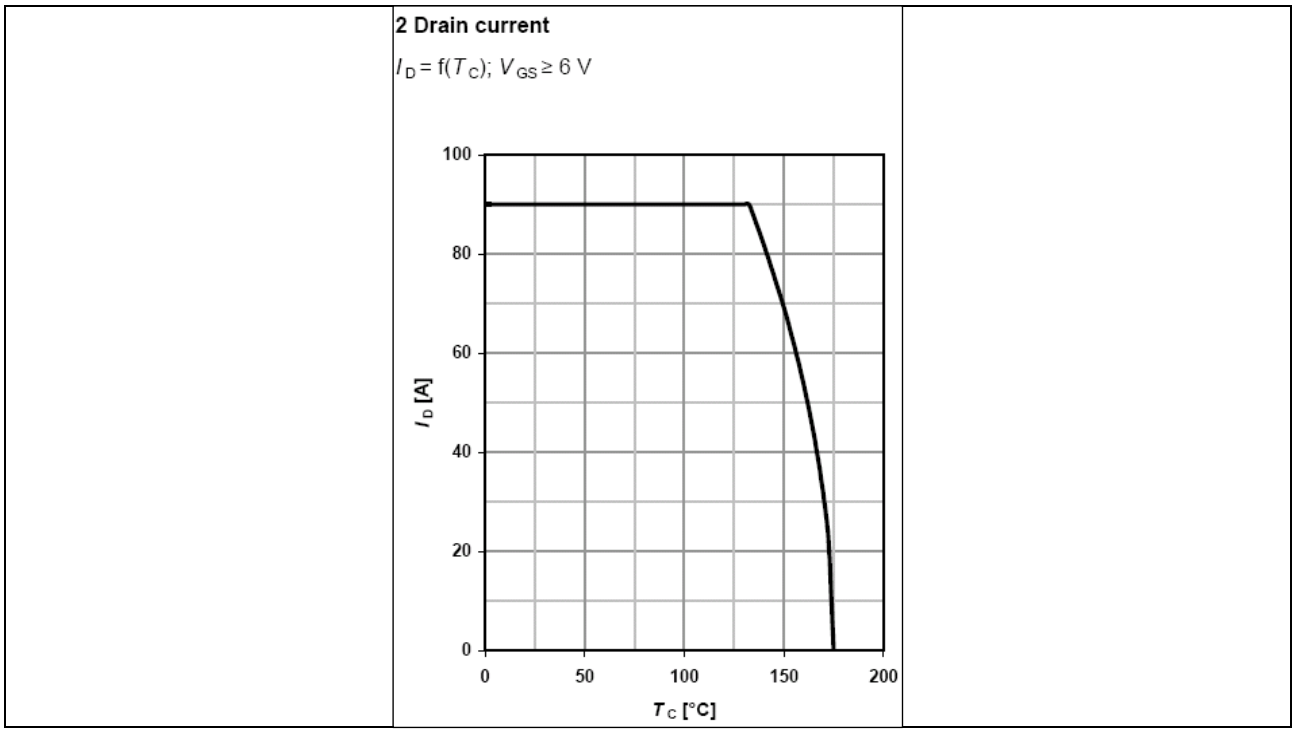

Figure 4 Drain current I_D = f(T_C)

3.3 Safe operating area

This diagram shows the drain current I_D as a function of the drain-source voltage V_{DS} with the condition of different pulse lengths.

There are several limitations in this diagram:

A) The top limit is related to the maximum pulsed drain current.

B) This area is limited by the on-state resistance $R_{DS(on)}$ at maximum junction temperature.

C) In this area a so-called constant power line will be observed. Depending on the pulse length of the applied power pulse, the thermal impedance changes and leads to different maximum power losses. For a given pulse length, the thermal impedance Z_{thJC} has to be determined by looking at the diagram “Maximum transient thermal impedance” (chapter 3.4).

$$(4) \quad I_D(V_{DS}) = \frac{T_J - T_C}{V_{DS} * Z_{thJC}}$$

D) In linear operations there is a risk for getting hot spots at low gate-source voltages due to the negative temperature characteristic in the transfer characteristic. This effect becomes more important for latest trench technologies with high current densities, where the “zero temperature coefficient” point of the transfer characteristic is shifted to higher drain currents. For more details please refer to application note “Automotive MOSFETs in Linear Applications: Thermal Instability”, available at www.infineon.com .

In order to consider the hot spot effect for higher VDS and longer pulse times, the SOA characteristic is showing a different slope in that region.

E) The maximum breakdown voltage $V_{(BR)DSS}$ is determined by the technology and limits the diagram on the right hand side.

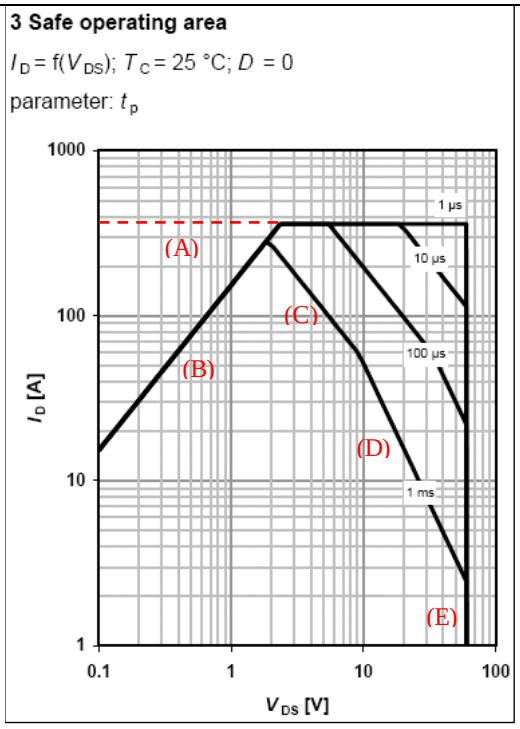

Figure 5 Safe operating area $I_D=f(V_{DS})$

3.4 Maximum transient thermal impedance Z_{thJC}

R_{thJC} is the thermal resistance from the junction of the die to the outside of the device. The heat is generated by the power loss in the device itself and the thermal resistance relates how hot the chip gets relative to the case.

Transient thermal impedance takes into account the heat capacity of the device, so it can be used to estimate directly temperatures resulting from power loss on transient base.

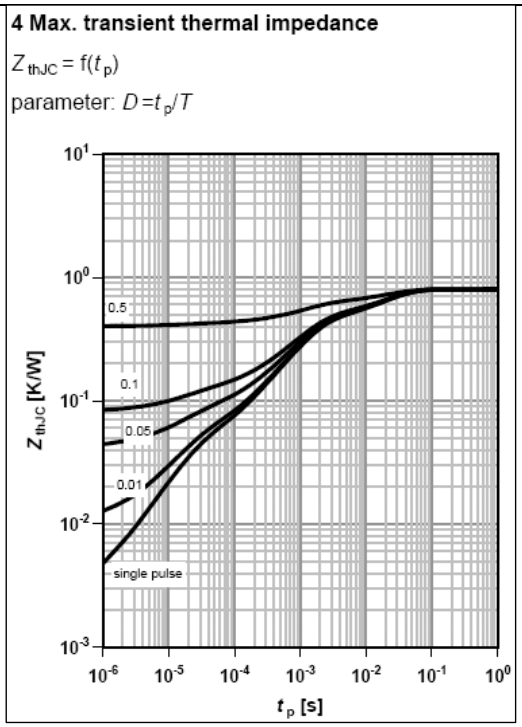

Figure 6 Maximum transient thermal impedance $Z_{thJC}=f(t_p)$

The diagram (Figure 6) shows the variation of the thermal resistance Z_{thJC} for the specified pulse duty factor $D=t_p/T$ as a function of the loading time t_p (pulse width).

To dissipate the heat out of the device, it has to pass several different layers with its characteristic thermal resistances and thermal capacitances. This results in the fact that depending on the pulse length either the thermal resistance or the thermal capacitance is dominating the behavior of the device. The increase of the junction temperature can be calculated as shown in equation (5). In a thermal equilibrium before applying the power pulse is $T_{J,start} = T_C$.

$$T_J = T_{J,start} + \Delta T_J = T_{J,start} + Z_{thJC}(t_P, D) * P_{tot} \quad (5)$$

Thermal characteristics[2)]

Thermal resistance, junction - case	R_{thJC}		-	-	0.8	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[3)]	-	-	40	

Figure 7 Thermal characteristics

3.5 Typical output characteristics

Those characteristic (Figure 8) is showing the typical dependence of the drain current I_D as function of the drain-source voltage V_{DS} at a given gate-source voltage V_{GS}. The chip temperature T_J is specified as well.

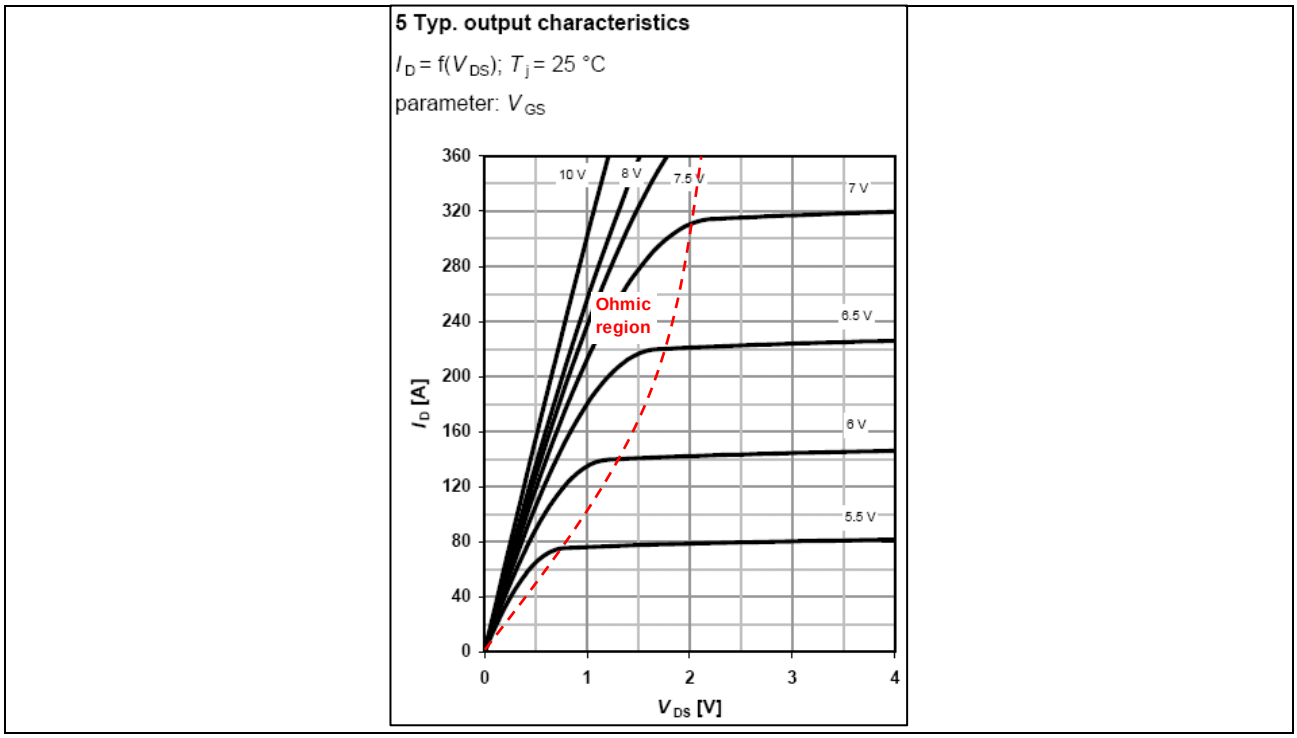

Figure 8 Typical output characteristics $I_D=f(V_{DS})$

The MOSFET should be operated in the “ohmic” region as shown in Figure 8. There is a maximum drain current for a corresponding gate-source voltage that a MOSFET will conduct. If the operating point at a given gate-source voltage goes above the “ohmic”region, any further increase in drain current leads to a significant rise in drain-source voltage (linear operation mode) and a consequent rise in conduction loss. If the power dissipation will not be limited in value and time, the device might be failing.

3.6 Drain-source on-state resistance as a function of Drain current

The Drain Source on-state resistance as a function over the Drain current with Gate Source voltage as a parameter can be directly calculated out of the typical output characteristic diagram.

$$R_{DS(on)}(I_D) = \frac{V_{DS}}{I_D} \quad (6)$$

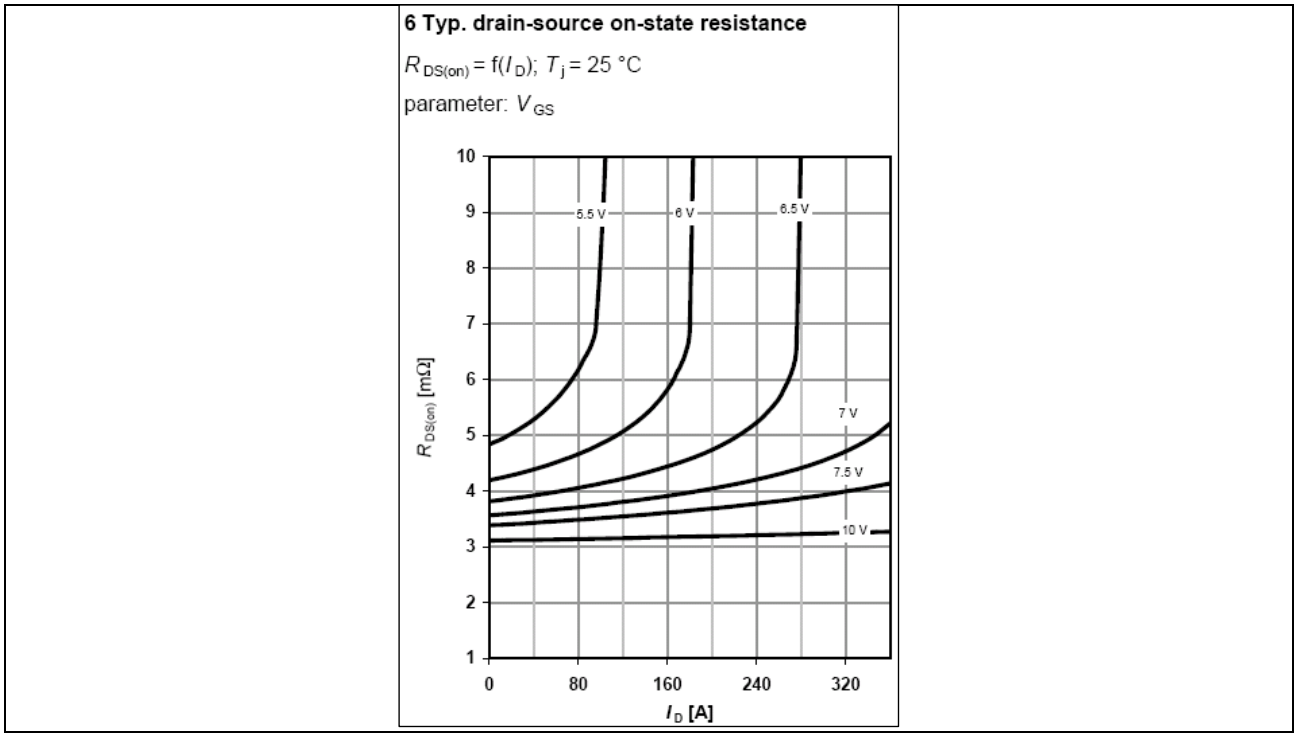

Figure 9 Typical drain-source on-state resistance $R_{DS(on)}$=f(I_D)

3.7 Transfer characteristics

This diagram is showing the typical Drain current as a function of the applied Gate to Source voltage. The graph is given at three different junction temperatures. Normally all the graphs are intersecting at one point, the so called temperature stable operating point.

If the Gate to Source voltage applied to the MOSFET is below that point (in the example V_{GS} < 6.2V), the MOSFET will operate with a positive temperature coefficient, meaning with increased junction temperature, the Drain current will increase as well. This operation condition is not preferable due to a possible thermal runaway.

Above the temperature stable operation point, the temperature coefficient is negative, meaning with increasing junction temperature the Drain current decreases. The MOSFET will limit its current handling capability at high temperatures itself. The operation in that range is uncritical (as long as the junction temperature stays within specification).

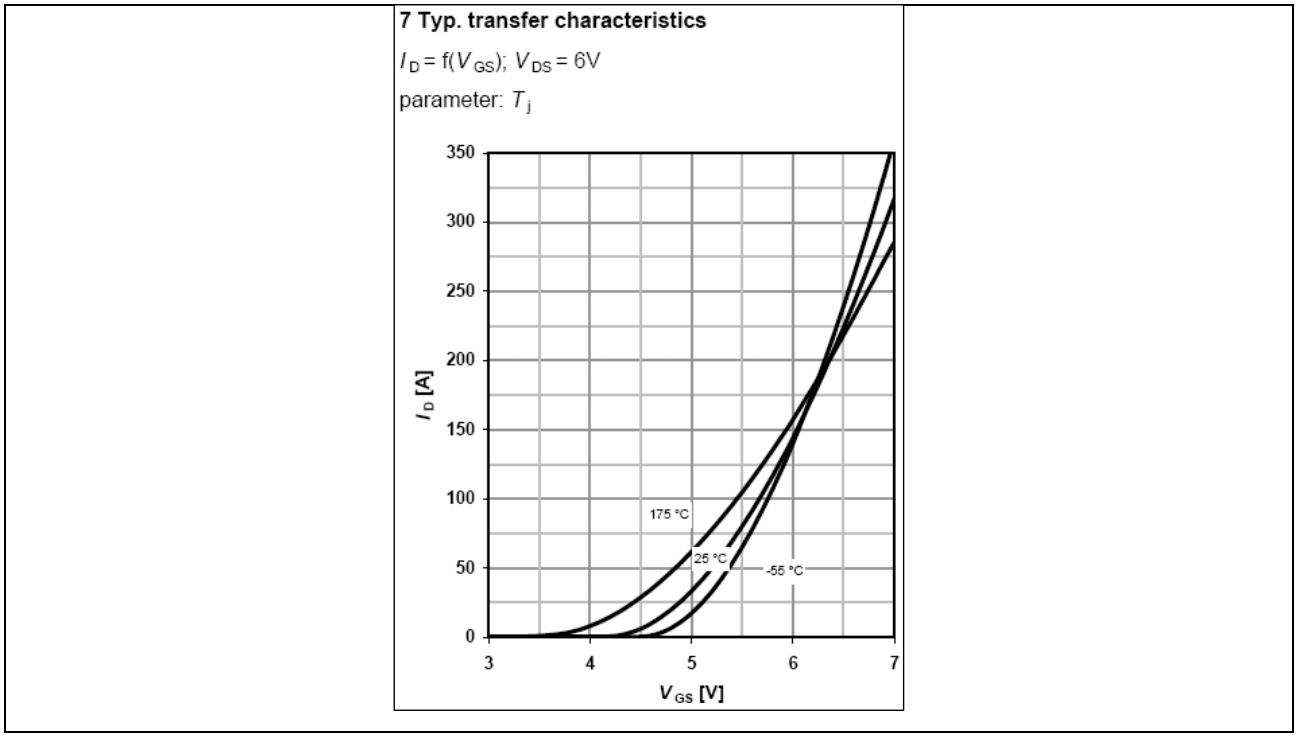

Figure 10 Typical transfer characteristics $I_D=f(V_{GS})$

To have a first idea about the max or min rating of that behavior, the curves can be moved in parallel according the min and max ratings of the threshold voltage (for a normal level device +/- 1V).

3.8 Drain-source on-state resistance

The drain-source on-state resistance is one of the key parameters of a MOSFET. In the data sheet there are two sections dealing with this resistance. In the table of the data sheet, typ. and max ratings at room temperature are given. This value is tested during production at the specified conditions.

For data sheets including Trough Hole and SMD devices, the R_{DSon} is separately mentioned. For an SMD device the resistance is measured between the Source Pin and the Drain backside of the device. For a Trough Hole package, the R_{DSon} is specified between the Drain and Source Pin of the package at a defined soldering point (for TO-220 approximately 4.5 mm lead lengths) resulting in a resistance adder of 0.3mOhm.

Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=90A	-	3.3	4	mΩ
		V_{GS}=10V, I_D=90A, SMD version	-	3.0	3.7	

Figure 11 Drain to Source on-state resistance

In addition to the table, the data sheet contains a diagram of the on-state resistance as a function of the junction temperature. The higher the junction temperature, the higher the R_{DSon} will be. Due to this positive temperature coefficient, it is easy to switch several devices in parallel.

The diagram is shown for typical R_{DSon} values only.

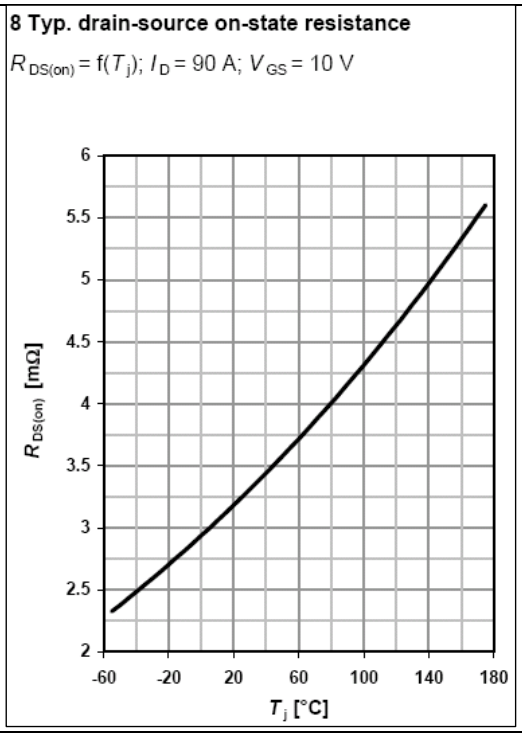

Figure 12 Typical drain-source on-state resistance $R_{DS(on)}$=f(T_j)

To calculate the dependency of the junction temperature following formula has to be taken:

$$R_{DSon}(T_J) = R_{DSon\_25°C} \cdot (1 + \frac{\alpha}{100})^{T_J - 25°C} \quad (7)$$

α is a technology related constant. For an approximation an alpha value of 0.4 can be taken for power MOSFETs.

3.9 Gate threshold voltage

The Gate Source threshold voltage defines the required Gate to Source voltage at a defined Drain current. During production the threshold voltage is measured at room temperature, with V_{DS} = V_{GS} and an area dependent Drain current in the µA range. The value is specified in the table with min, typ. and max ratings.

Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=90µA	2.0	3.0	4.0	

Figure 13 Threshold voltage

Due to the fact that the threshold voltage decreases for increasing junction temperatures this dependency is specified for typical values in a diagram.

For high junction temperatures, the Drain current can already reach the leakage current (I_{DSS}) of the MOSFET, therefore an additional curve with ten times higher Drain currents compared to the table specification is defined.

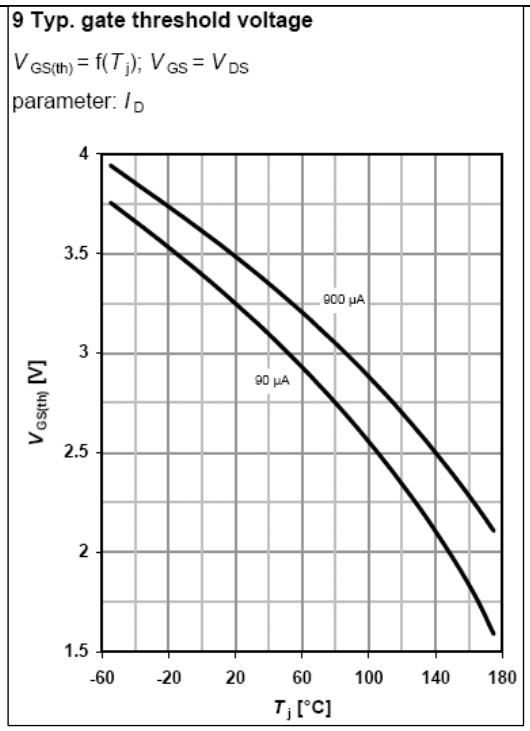

Figure 14 Typical gate threshold voltage $V_{GS(th)}$=f(T_j)

3.10 Capacitances

The capacitances of the MOSFETs are defined on the one hand in the table section of the data sheet but as well as a diagram due to their dependencies of the Drain to Source voltage.

These parameters are not tested during production, the max values are derived from production variants, which were investigated during the development of the device in detail.

Because it is not possible to measure some capacitances directly, the Gate to Source etc. capacitances can be calculated out of the defined values accordingly.

$$C_{iss} = C_{GS} + C_{GD}$$
$$C_{oss} = C_{DS} + C_{GD} \quad (8)$$
$$C_{rss} = C_{GD}$$

Dynamic characteristics[2)]

Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	7980	10400	pF
Output capacitance	C_{oss}		-	1960	2540	
Reverse transfer capacitance	C_{rss}		-	75	150	

Figure 15 Dynamic characteristics: capacitances

In the diagram area of the data sheet the typical capacitances as a function of the Drain to Source voltage are defined. Especially the reverse (C_{rss}) and output (C_{oss}) capacitances are showing extreme dependencies over the voltage. Reason for that is the change in the space charge region during the switching transition of the MOSFET.

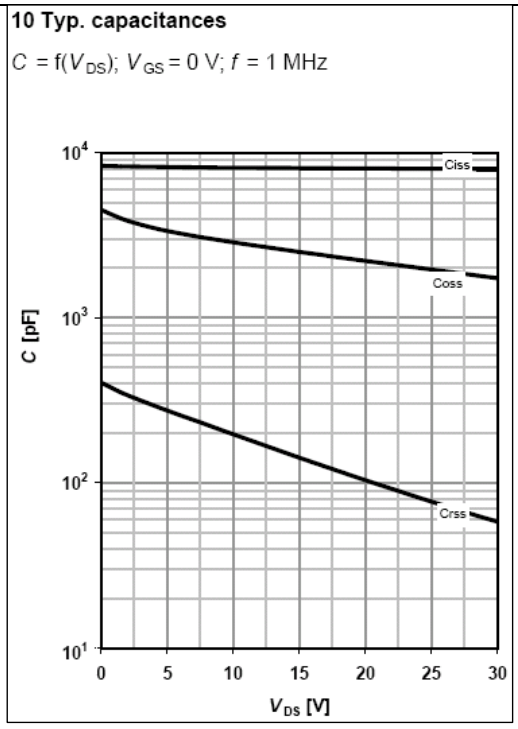

Figure 16 Capacitance C=f(V_{DS})

3.11 Reverse diode characteristics

The characteristics of the MOSFET's internal diode are given twofold. First in the table part, as in Figure 17, second as a diagram (Figure 19) with the typical forward diode characteristics $I_F = f(V_{SD})$ at two different junction temperatures: $T_J = 25°C$ and $T_J = 175°C$.

- Diode continuous forward current: The maximum permissible DC forward current of the inverse diode at the specified case temperature $T_C = 25°C$ (normally equal to the MOSFET's continuous current).
- Diode pulse current: The maximum permissible pulsed forward current of the inverse diode at the specified case temperature $T_C = 25°C$ (normally equal to the MOSFET's pulse current).
- Diode forward voltage: A voltage at diode on-state (MOSFET off-state) across the source and the drain terminals at given diode forward current I_F, given voltage V_{GS} = 0V and given junction temperature $T_J = 25°C$.
- Reverse recovery time: The time needed for the reverse recovery charge to recombine. The graphical explanation of t_{rr} is given in Figure 18.
- Reverse recovery charge: The charge stored in the diode during its on-time and being absorbed by another switching device (e.g. MOSFET in the same leg in a bridge configuration). The graphical explanation of t_{rr} is given in Figure 18.

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Reverse Diode						
Diode continous forward current[2)]	I_S	T_C=25°C	-	-	90	A
Diode pulse current[2)]	$I_{S,pulse}$		-	-	360	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=90A, T_j=25°C	0.6	0.95	1.3	V
Reverse recovery time[2)]	t_{rr}	V_R=30V, I_F=50A, di_F/dt=100A/µs	-	125	-	ns
Reverse recovery charge[2)]	Q_{rr}		-	110	-	nC

Figure 17 Diode characteristics

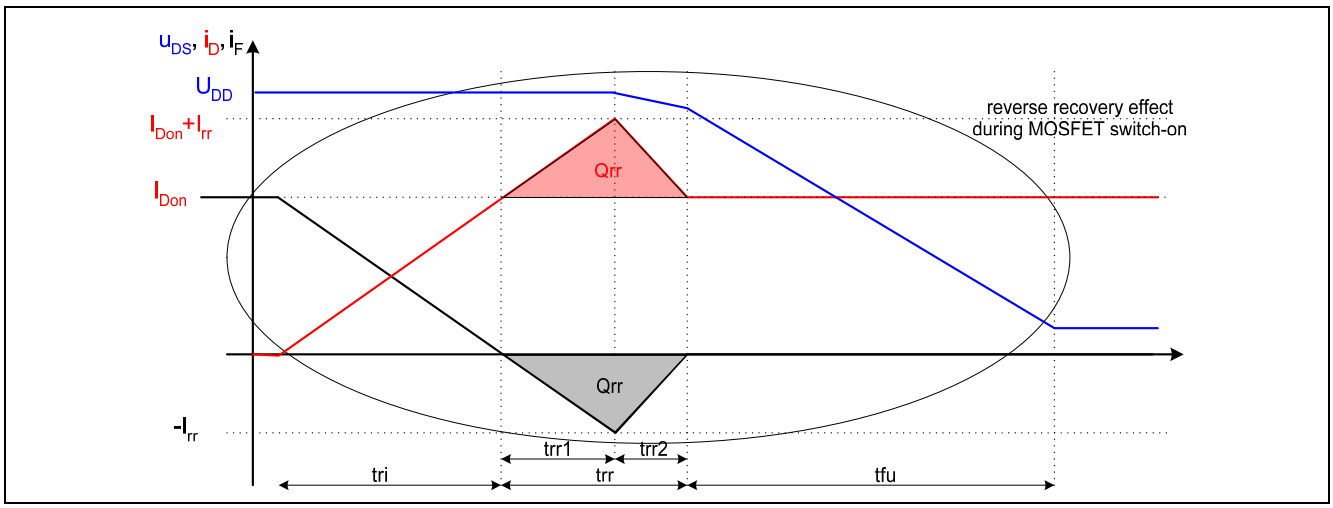

Figure 18 Explanation of Q_{rr} and t_{rr}

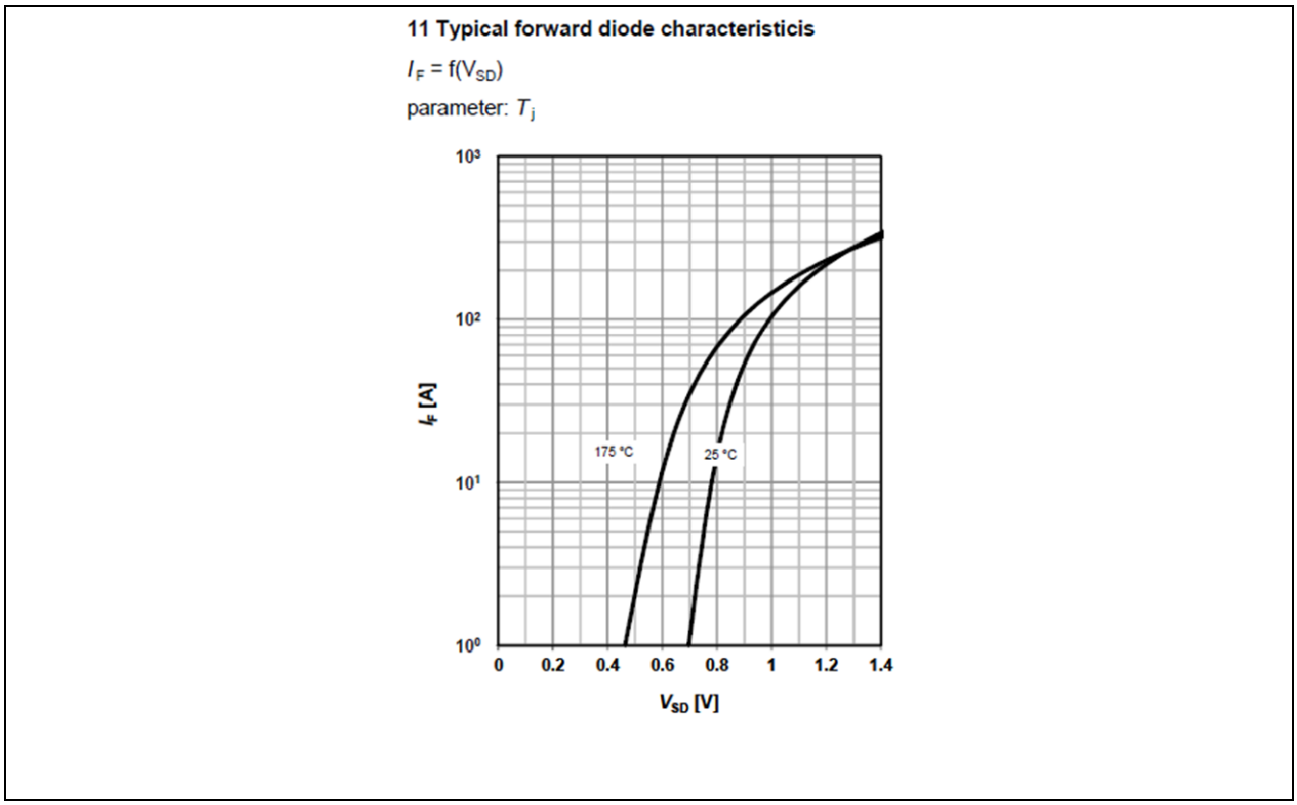

Figure 19 Typical forward diode characteristics $I_F=f(V_{SD})$

3.12 Avalanche characteristics

The dependence of the pulsed avalanche current I_{AV} on the time in avalanche t_{AV} is presented in Figure 20. Operation of the MOSFET below the curve, under consideration of the maximum junction temperature in pulsed avalanche, is allowed. For the same avalanche energy, if the current decreases, the time in avalanche would increase. Additional parameter in the figure is the junction temperature at the beginning of the avalanche event. The increase of temperature leads to decrease of the avalanche capability.

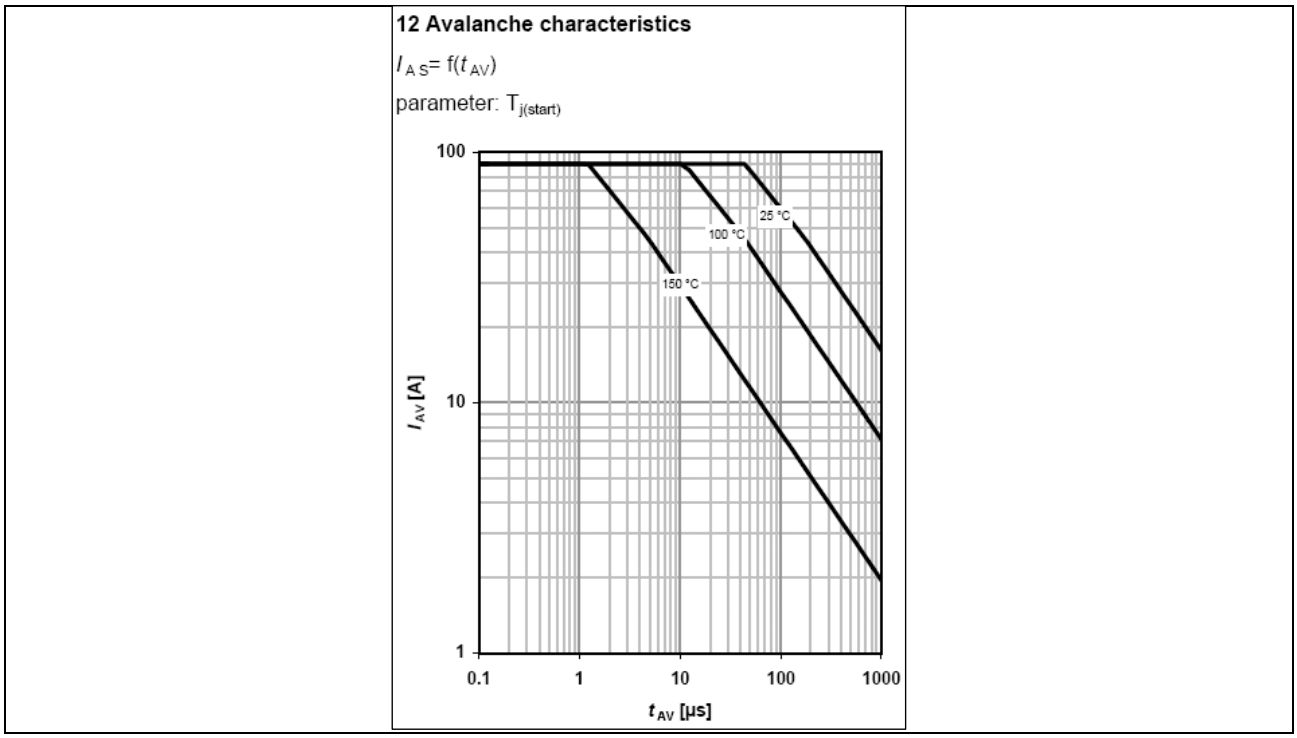

Figure 20 Avalanche characteristics $I_{AS}=f(t_{AV})$

3.13 Avalanche energy

The table part of the datasheet gives information on the maximum avalanche energy at given avalanche current, as well as the maximum current in avalanche.

Avalanche energy, single pulse[2)]	E_{AS}	I_D=45A	331	mJ
Avalanche current, single pulse	I_{AS}		90	A

Figure 21 Avalanche energy and current

The diagram in Figure 22 shows the variation of the maximum single-pulse avalanche energy E_{AS} as a function of chip temperature at a given avalanche current. With increasing junction temperature the avalanche power handling capability decreases according to:

$$E_{AS}(T_J) = \left(\frac{T_{J\_max} - T_J}{T_{J\_max} - 25^oC} \right)^2 * E_{AS\_25^oC} \quad (9)$$

This formula is valid for the specified avalanche current only. By varying the avalanche current, the diagram would show different results. As a rule of thumb the avalanche power handling capability is inversely proportional to the avalanche current.

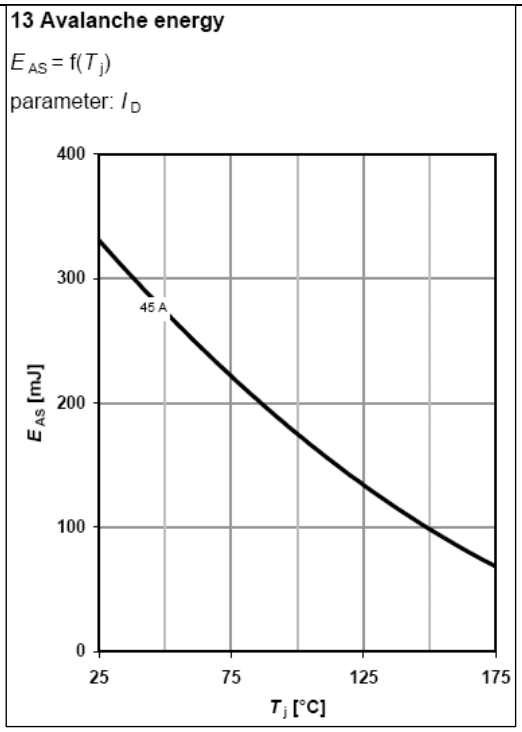

Figure 22 Avalanche energy $E_{AS}=f(T_j)$

3.14 Drain-source breakdown voltage

The diagram in Figure 23 gives the typical dependency of the minimum value of the drain to source breakdown voltage over the whole temperature range (-55°C…+175°C). The table value, as given in Figure 24 gives the min value of the breakdown voltage at 25°C.

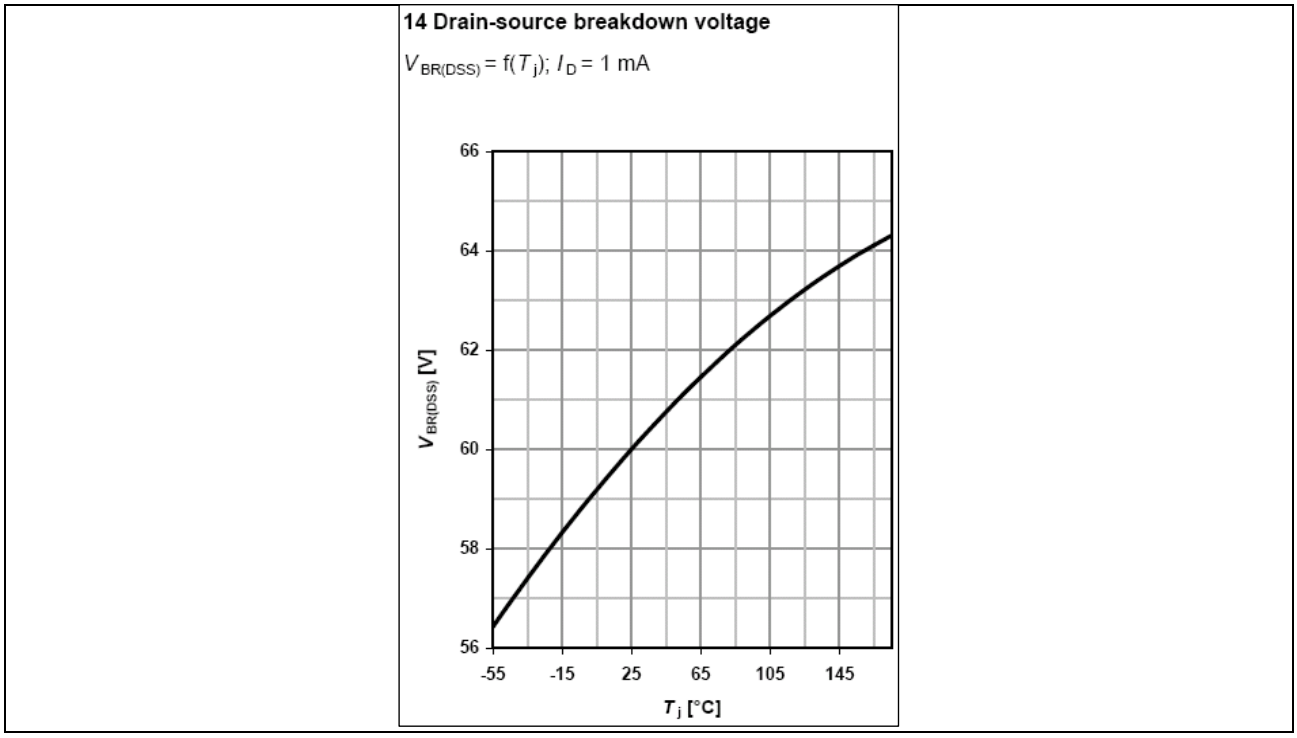

Figure 23 Drain-source breakdown voltage $V_{BR(DSS)}$=f(T_j)

Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	60	-	-	V

Figure 24 Drain-source breakdown voltage $V_{BR(DSS)}$ @ 25°C

3.15 Typical gate charge

The diagram shows the typical variation of the requisite gate charge at the given gate source voltage and drain-source supply voltage for switching on a power MOSFET. The on state current is given as a parameter.

The gate charge comprises the charge Q_{GS}, which is required for charging the gate-source capacitance C_{GS}. During this phase, after the gate threshold voltage $V_{GS(th)}$ has been reached, the drain current rises to its specified value, and the drain source voltage then falls (it can happen simultaneously for the resistive loads or after one another with the inductive loads). Until the voltage V_{DS} has fallen to its actual on-state value (V_{DS} = R_{DSon}·I_D), the gate-to-drain capacitance (Miller capacitance) has to be discharged. This charge component is defined as the gate-to-drain charge Q_{GD}. The charge Q_{GS} + Q_{GD} is not sufficient to fully switch the transistor on, since the drain-source on-state resistance has not yet been minimized. Only with a charge corresponding to a full gate source voltage is the full turn-on resistance reached, and thus static losses, optimized. This whole charge Q_G depends on the drain-source voltage (or the supply voltage) that has to be switched. The charge values are also summarized in the table part as shown in Figure 26.

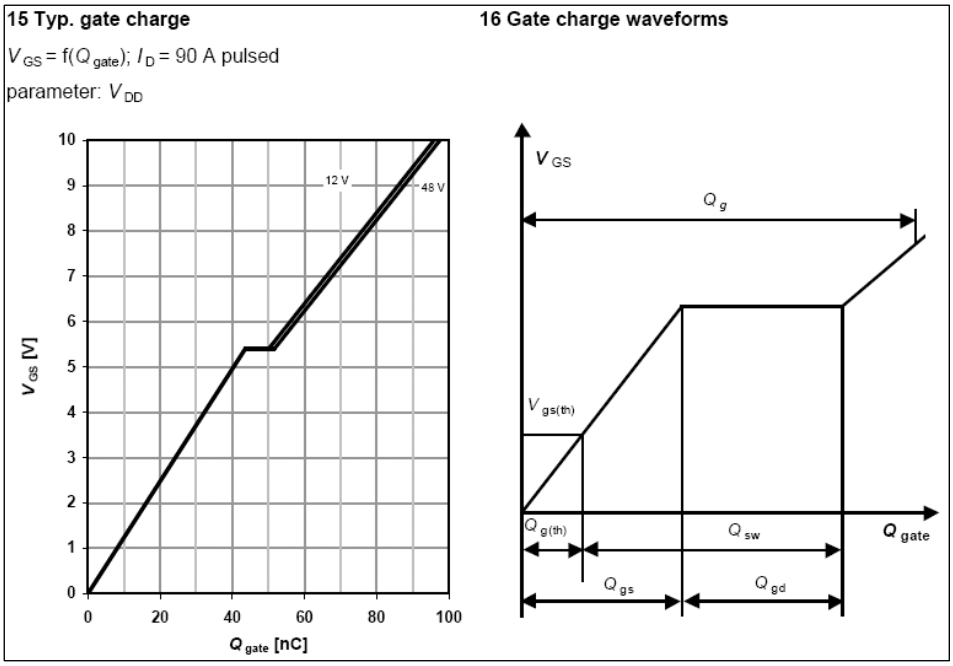

Figure 25 Typical gate charge V_{GS} = f(Q_{gate}) and gate charge waveforms

Gate Charge Characteristics[2)]

Gate to source charge	Q_{gs}	V_{DD}=48V, I_D=90A, V_{GS}=0 to 10V	-	44	57	nC
Gate to drain charge	Q_{gd}		-	10	20	
Gate charge total	Q_g		-	99	128	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V

Figure 26 Gate charge and plateau voltage

3.16 Leakage Currents

There are two leakage currents specified for a MOSFET:

I_{DSS} is the drain-source leakage current at a certain drain-source voltage (typically the minimum drain-source breakdown voltage) and at V_{GS}=0V.

I_{GSS} is the gate-source leakage current at a certain gate-source voltage (typically the max. gate-source voltage) and at V_{DS}=0V.

Zero gate voltage drain current	I_{DSS}	V_{DS}=60V, V_{GS}=0V, T_j=25°C	-	0.01	1	µA
		V_{DS}=60V, V_{GS}=0V, T_j=125°C[2)]	-	5	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA

Figure 27 Leakage Currents

3.17 Switching Times

The turn-on time, t_{on}, of a MOSFET is the sum of the turn-on delay time $t_{d(on)}$ and the rise time t_r. $t_{d(on)}$ is measured between the 10% value of the gate-source voltage and the 90% value of the drain-source voltage. The rise time t_r is measured between the 90% value and the 10% value of the drain-source voltage.

The turn-off time, t_{off}, of a MOSFET is the sum of the turn-off delay time $t_{d(off)}$ and the fall time t_f. $t_{d(off)}$ is measured between the 90% value of the gate-source voltage and the 10% value of the drain-source voltage. The fall time t_f is measured between the 10% value and the 90% value of the drain-source voltage.

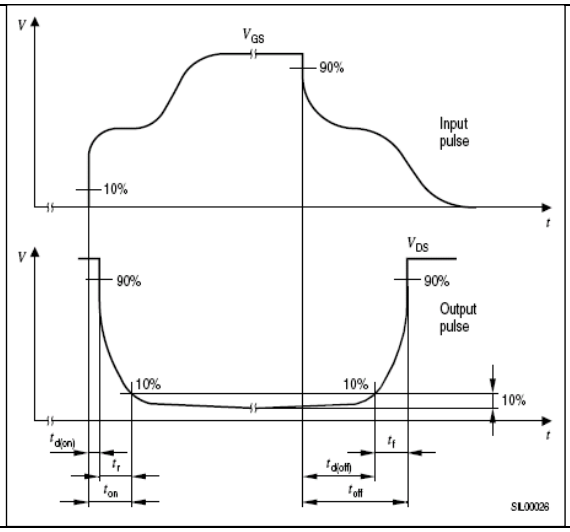

Figure 28 Definition of switching times

Turn-on delay time	$t_{d(on)}$	V_{DD}=30V, V_{GS}=10V, I_D=90A, R_G=3.5Ω	-	30	-	ns
Rise time	t_r		-	70	-	
Turn-off delay time	$t_{d(off)}$		-	40	-	
Fall time	t_f		-	5	-	

Figure 29 Switching Times

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