Application Note AN-1194

Using MOSFET Spice Models for Analyzing Application Performance

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Uses for MOSFET Spice Models

As design cycle times get shorter, which has always been the case, tools are needed to help the engineer meet this challenge. Circuit simulation in the form of Spice is a tool that can help in selecting the right topology and the accompanying MOSFET. Spice can be used to calculate MOSFET power dissipation, predict gate drive performance, circuit avalanche energy, switching times, estimate short time duration transient junction temperature increase and much more. Given that there are low cost or free versions of Spice available and that International Rectifier provides spice models for MOSFETs on the web site, circuit simulation is readily available to all power engineers.

Another way at looking at the value of using circuit simulation is to consider that it can be used to answer design questions like:

- Which MOSFET can I use to meet price performance requirements?
- What gate driver should I use? How should it be configured?
- How do I heatsink the MOSFET? What heatsink do I use? What Cu weight should I choose for my surface mount board?
- Can I use the MOSFET as an inductive clamp or do I need to add an external catch diode?
- Will the MOSFET experience dv/dt turn-on in a half-bridge circuit?
- Etc

With these and other questions being answered the engineer can make informed design decisions up front reducing the potential number of respins of the product before launch.

MOSFET Spice Model Availability

For each new MOSFET that is released by International Rectifier a corresponding Spice model is generated and published. The model comes in the form of a text file that can be imported into the spice program. Just search www.irf.com for a desired MOSFET and there will be link to its corresponding model.

Power MOSFET Spice Model

The power MOSFET Spice macro model is comprised of fundamental circuit elements plus the standard CMOS model. Figure 1 shows a simplified version of a Power MOSFET Macro model.

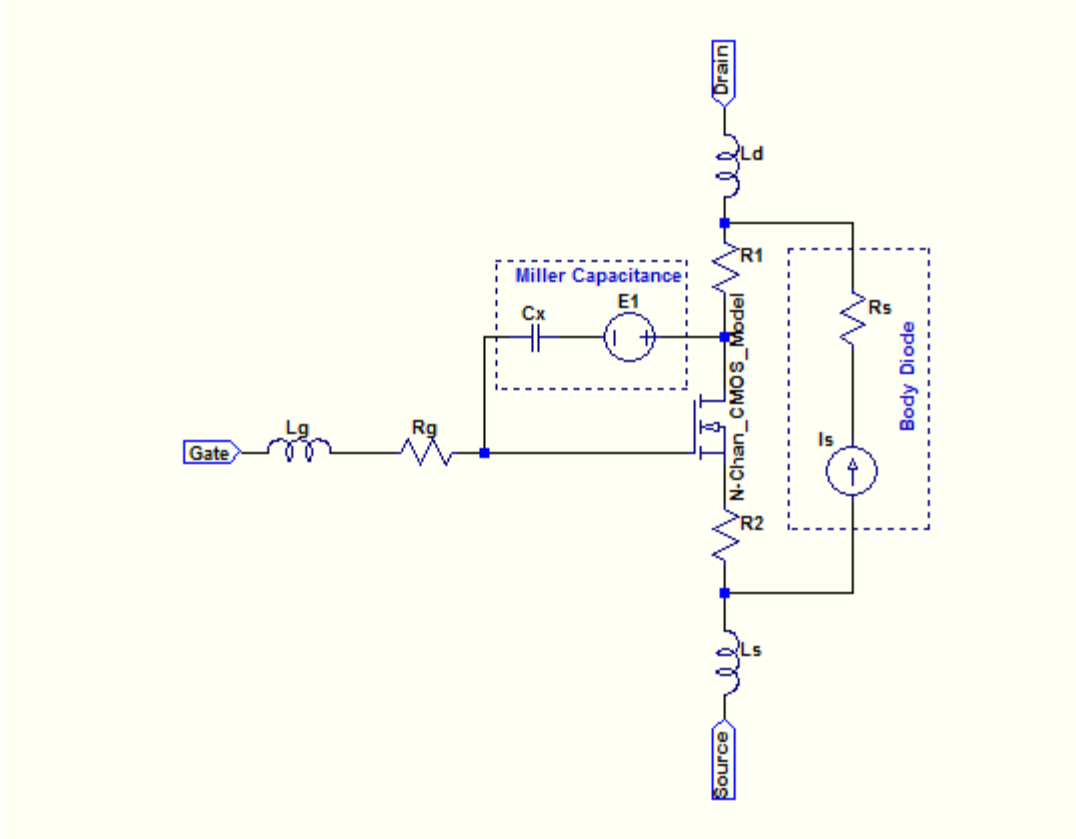

Figure 1: Simplified Power MOSFET Marco Model

Some elements in Figure 1 reflect actual physical aspects of the MOSFET and its package while other elements are there to realize physical behavior via circuit element constructs. The following describes the relationship between the model and the real MOSFET.

Lg: The gate lead and bond wire inductance
Rg: The internal series gate resistance (principally the polysilicon gate resistance).
Ld: The drain lead and bond wire inductance
R1: The epitaxial layer bulk resistance and drain lead resistance
Rs: The diode bulk resistance
Is: A non-linear current source representing the relationship between diode current and diode voltage
R2: The source lead and bond wire resistance
Ls: The source lead and bond wire inductance
Cx: A scaled value of capacitance used to simulate the effect of Cgd (Miller Capacitance)
CMOS Model: Implements the following equations

$$I_d = K\frac{W}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right](1 + \lambda V_{ds}) \qquad V_{gs} > V_t, V_{ds} \leq V_{gs} - V_t$$

$$I_d = \frac{1}{2}K\frac{W}{L}(V_{gs} - V_t)^2(1 + \lambda V_{ds}) \qquad V_{gs} > V_t, \quad V_{ds} > V_{gs} - V_t$$

Note: The simplified model here does not include diode reverse recovery. However the posted models have reverse recovery included.

The parameters of this model for a given MOSFET part number are determined using the MOSFET characterization data and curve fitting software. Both curves (Ciss, Coss, Crss, Drain-Source Diode IV curve, Vgs vs Qg etc) and particular measured values like BVdss, Rdson etc are entered into the software. The software performs curve fitting which results in a set of model parameters that allow the macro model to recreate the original characterization data using test circuits. The following is an example of a MOSFET Spice model that can be found on www.irf.com .

```
.SUBCKT irfh5006pbf 1 2 3
* SPICE3 MODEL WITH THERMAL RC NETWORK
**************************************
*      Model Generated by MODPEX     *
*Copyright(c) Symmetry Design Systems*
*         All Rights Reserved        *
*    UNPUBLISHED LICENSED SOFTWARE   *
*   Contains Proprietary Information *
*      Which is The Property of      *
*     SYMMETRY OR ITS LICENSORS      *
*Commercial Use or Resale Restricted *
*   by Symmetry License Agreement    *
**************************************
* Model generated on Aug 17, 10
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=3.71802 LAMBDA=0.0415081 KP=45.7788
+CGSO=4.01469e-05 CGDO=1.62897e-06
RS 8 3 0.0001
D1 3 1 MD
.MODEL MD D IS=2.80456e-09 RS=0.00116577 N=1.19518 BV=60
+IBV=0.00025 EG=1 XTI=2.19334 TT=1e-07
+CJO=4.29277e-09 VJ=0.5 M=0.640529 FC=0.5
RDS 3 1 1e+07
RD 9 1 0.0001
RG 2 7 1.78118
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=1.8337e-09 VJ=0.500012 M=0.819764 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.400109 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 2.01999e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
```

```
D4 0 6 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.400109
.ENDS irfh5006pbf
*SPICE Thermal Model Subcircuit
.SUBCKT irfh5006pbft 5 1

R_RTHERM1         5 4  3.93e-10
R_RTHERM2         4 3  0.025591
R_RTHERM3         3 2  0.164071
R_RTHERM4         2 1  0.310278
C_CTHERM1         5 1  1.56182e+11
C_CTHERM2         4 1  0.002251121
C_CTHERM3         3 1  0.004889843
C_CTHERM4         2 1  0.010577591

.ENDS irfh5006pbft
```

Figure 2: Spice Model of the IRFH5006

Notice at the end of the Spice model there is a thermal model (sub-circuit) that is rendered as a RC network. This Cauer network will allow for the realization of the single pulse thermal response on the Zthjc vs tpulse curve.

Spice Model Validation

As with all software tools that are used to simulate real world phenomena, the question of accuracy arises. At issue, is which aspects of the model are accurate and which are not.

Here are some limitations of the posted models:

- Models only behave as if the MOSFET is held at 25C during the entire simulation period. The behavior does not change as a function of temperature because there is no temperature dependence in the model. (Rdson, Vth, BVdss etc have no temperature dependencies)
- The model can't be used to create an SOA curve because the Thermal Instability effect is not modeled.
- Although the body diode reverse recovery is modeled it is not very accurate. It can give exaggerated reverse recovery current spikes.

The following shows a comparison between measured data and spice simulation results for a Double Pulse Test of the IRFH5006 (60V N-Channel 5x6 PQFN MOSFET). The purpose of choosing the Double Pulse test for this comparison is to select an operating scenario that does not induce MOSFET self-heating. Thus the MOSFET will behave as a 25C device throughout the duration of the measurement which is what is modeled in spice.

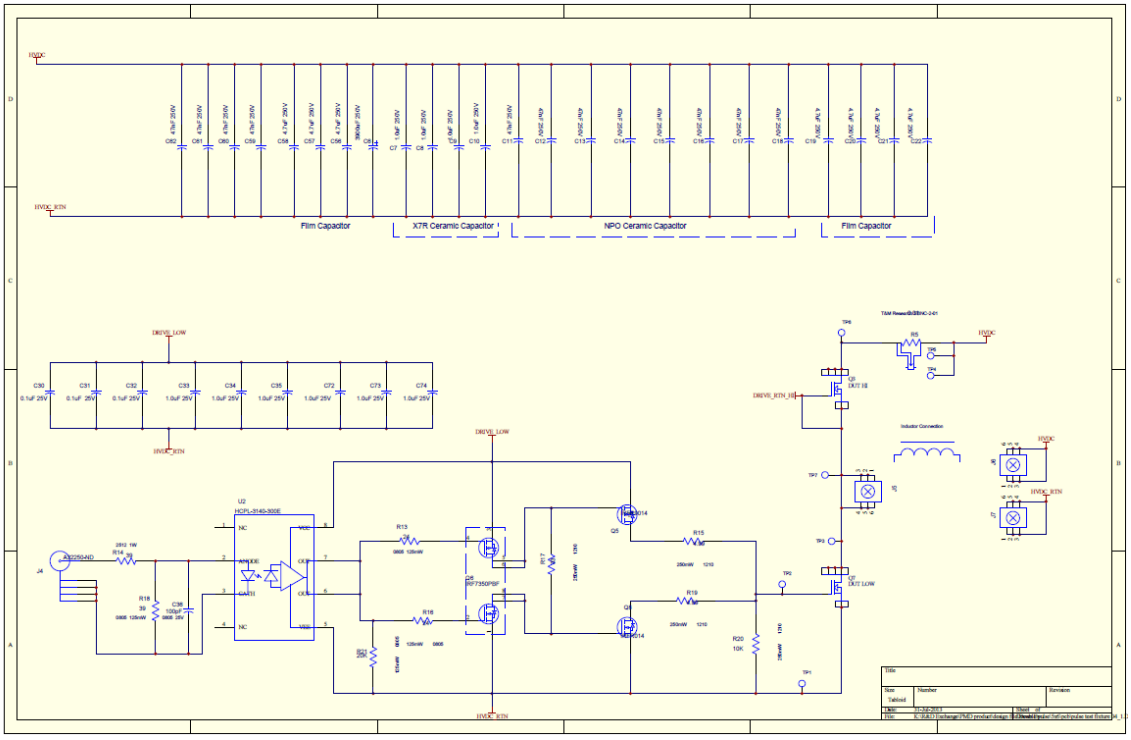

Figure 3 - Double Pulse Tester Schematic

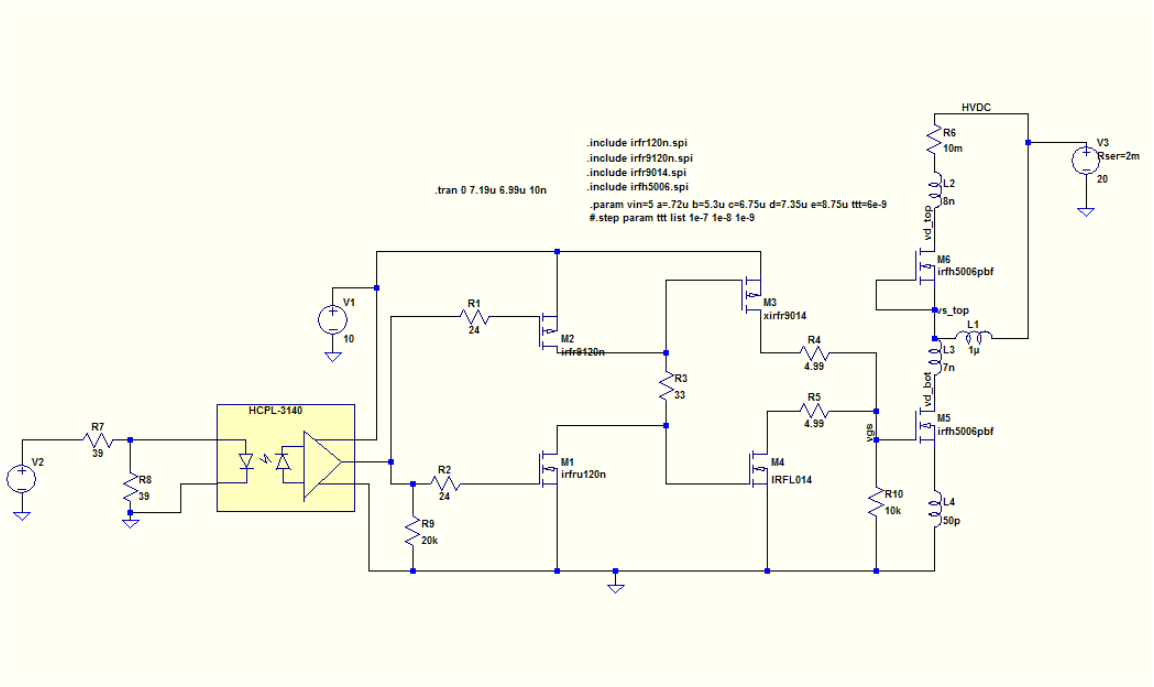

Figure 4 - Double Pulse Tester Simulation Schematic

In Figure 4 L2-L4 were added to mimic the board and probe parasitic inductances.

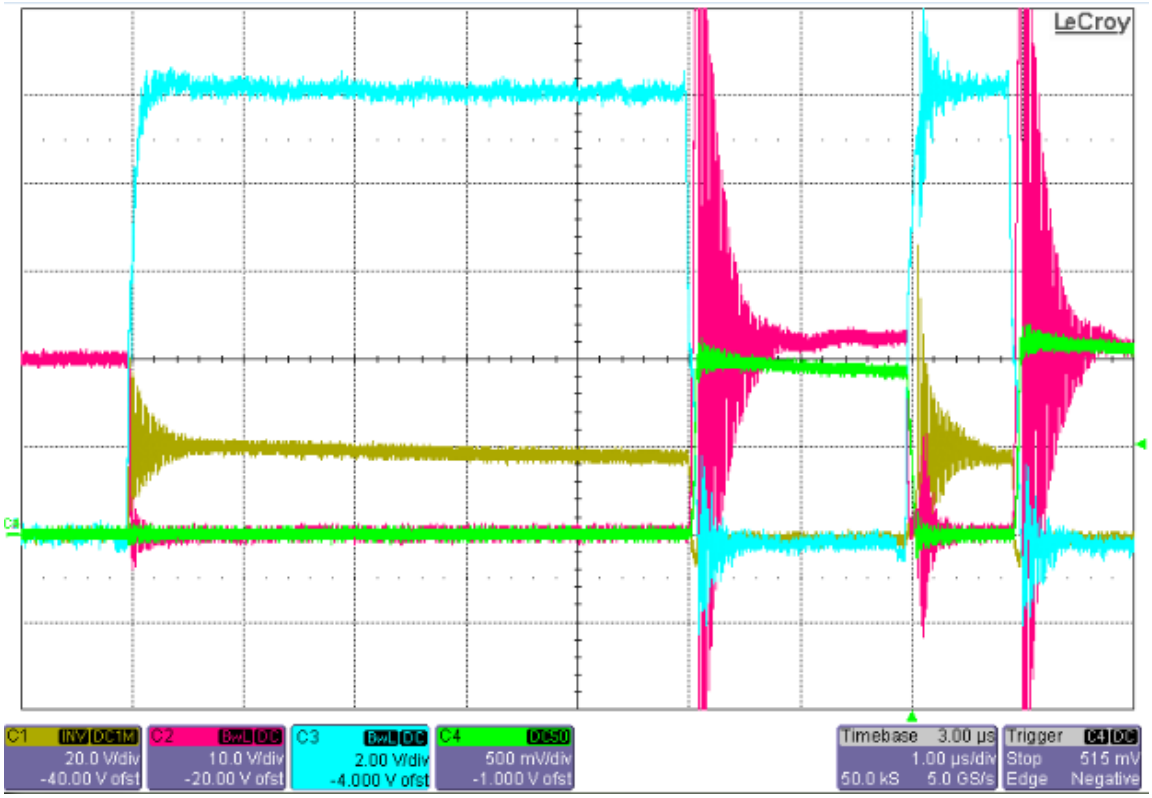

Figure 5 - Measured Double Pulse Test HVDC=20V

In Figure 5:
C1 (Dark Green color) – Upper FET's Vds
C2 (Red color) - Lower FET's Vds
C3 (Light Blue color) – Lower FET's Vgs
C4 (Green color) – Upper FET's Id

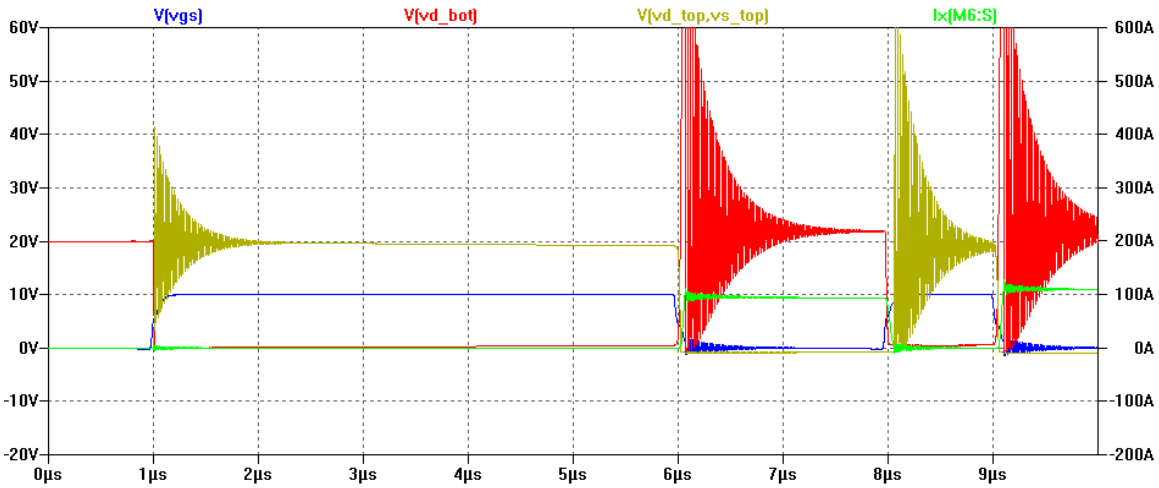

Figure 6 - Simulated Double Pulse Test HVDC=20V

In Figure 6:
V(vd_top,vs_top) - Upper FET's Vds
V(vd_bot) - Lower FET's Vds
V(vgs) - Lower FET's Vgs

Ix(M6:S) - Upper FET's Id

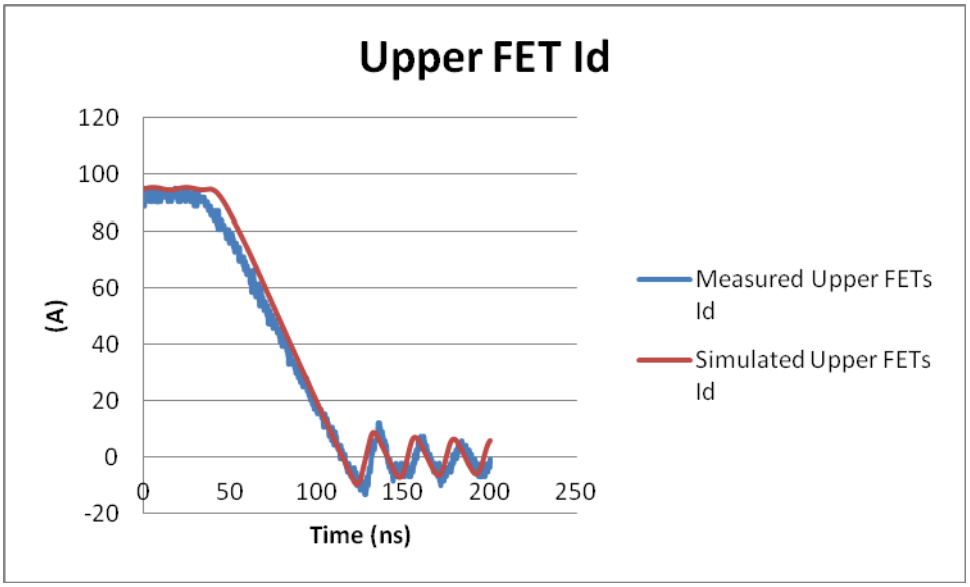

Figure 7 - Upper FET Id Comparison

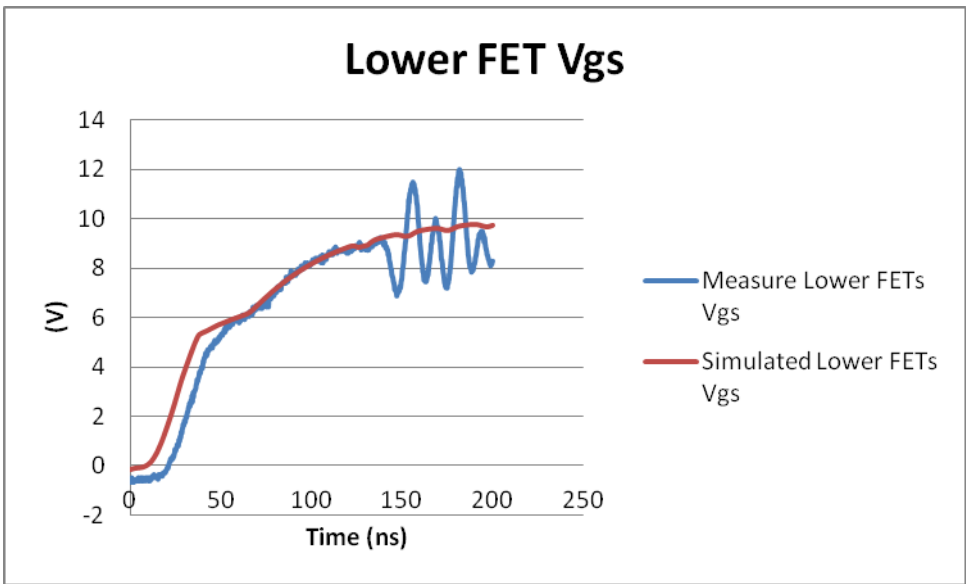

Figure 8 - Lower FET Vgs Comparison

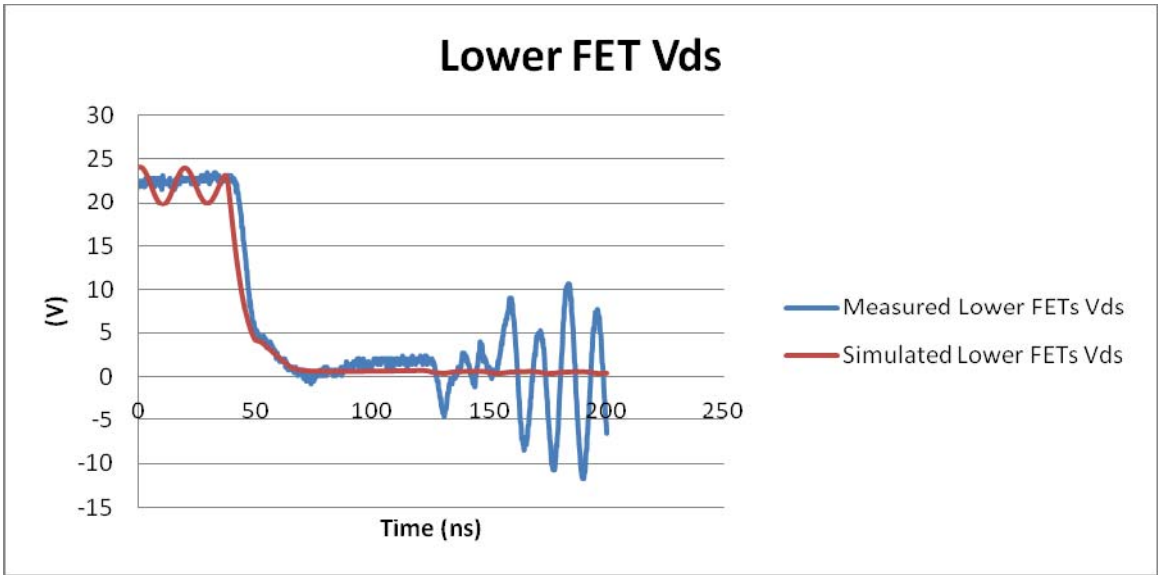

Figure 9 - Lower FET Vd Comparison

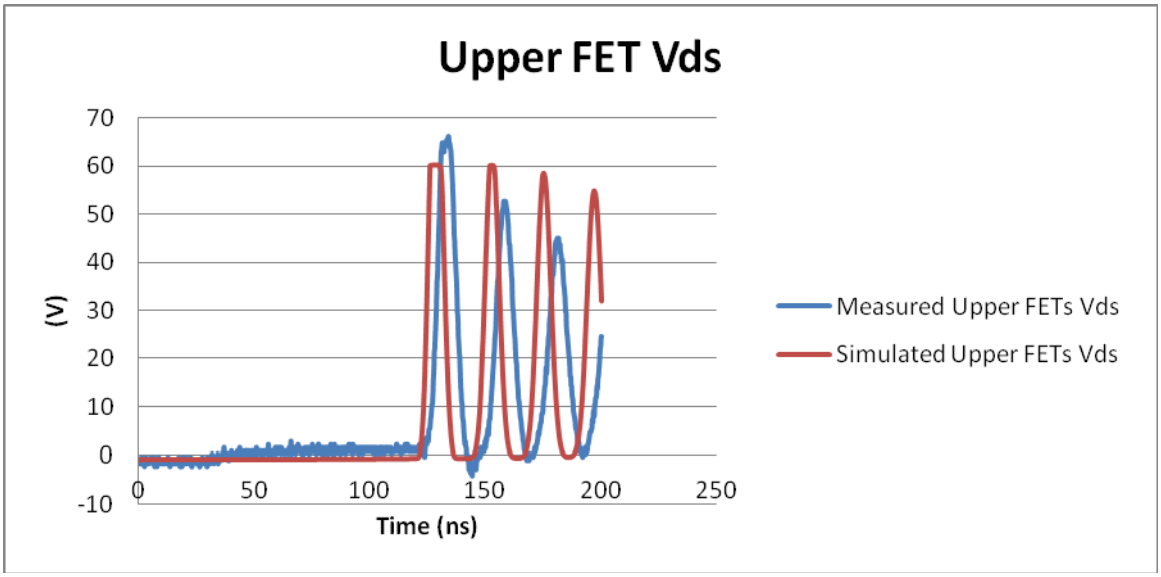

Figure 10 - Upper FET Vds Comparison

In addition to adding the parasitic inductance, the reverse transit time of the body diode in the IRFH5006 spice model had to be changed from tt=1e-7 to tt=6e-9.

Figures 7-10 demonstrate the validity of the spice model at the 10's of nanosecond level. What was not completely realized in the simulation are total parasitic effects of both the board layout and the scope probing. One important point to note about this simulation is that switching losses as well as conduction losses can be reasonability estimated using simulation.

MOSFET Design Validation Simulation Example

H-Bridge

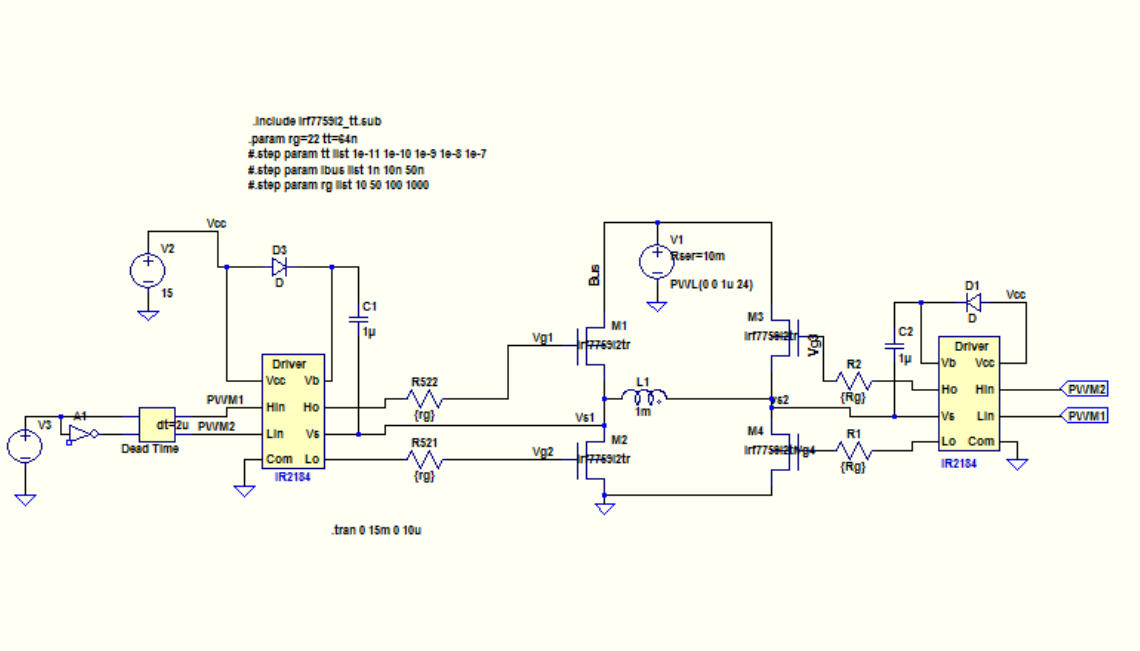

Figure 11: H-Bridge Simulation Model

Figure 3 shows an example of a MOSFET H-Bridge driving an L-R load. In this case:

Fsw=10KHz
Duty Cycle=80%/20%
Load Current is 25A
Rg=22Ω
Battery Voltage=24V
Deadtime=2us
Gate Driver is a macro model of the IR2184
MOSFETs are the IRF7759L2 DirectFET

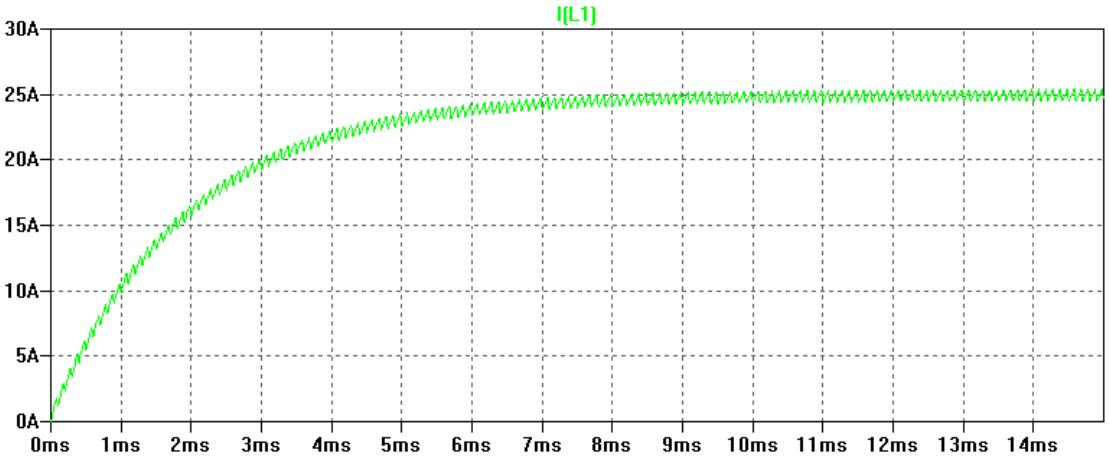

Figure 12: H-Bridge Load Current

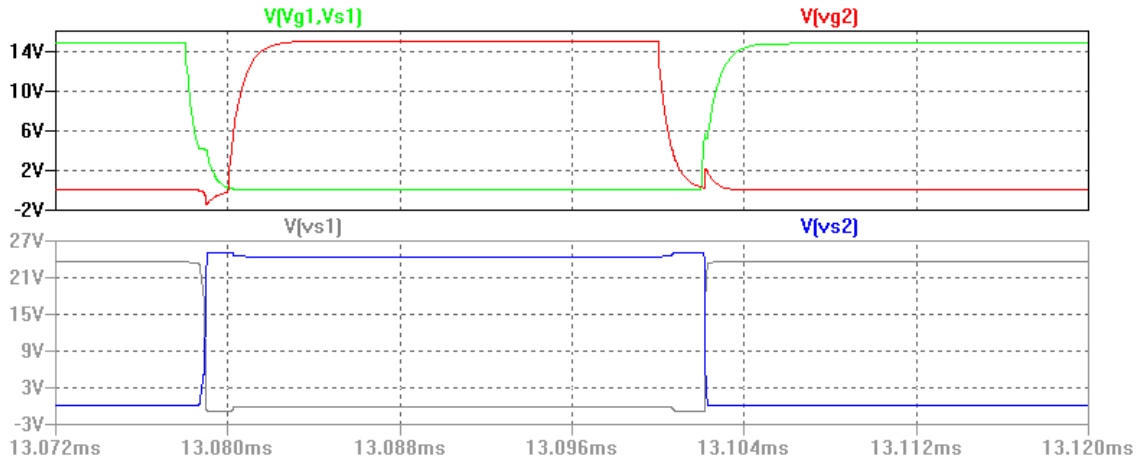

Figure 13: Gate drive and Switch Node Waveforms

Running a power measure analysis on the MOSFETs yields:

PowerM1=PowerM4=2.14W
PowerM2=PowerM3=0.74W

From this simulation analysis board layout and Cu weight decisions can be made. Also the interactions between the gate driver and MOSFET can be understood and the drive circuit can be optimized.

Summary

International Rectifier has MOSFET Spice models on www.irf.com that can be used for pre-prototype circuit validation for a multitude of power application topologies. Performing simulation is a low cost way to validate a design and make the appropriate trade-offs. The Spice models represent a guard banded version of the actual MOSFET. Conservative modeling yields a guard banded analysis, which is part of good design practices.

References and Acknowledgements

AN-975A Spice Computer Models HEXFET Power MOSFETs by S. Malouyans
Software: LTSpice IV Version 4.20b
MODPEX is copyrighted by Symmetry Design Systems